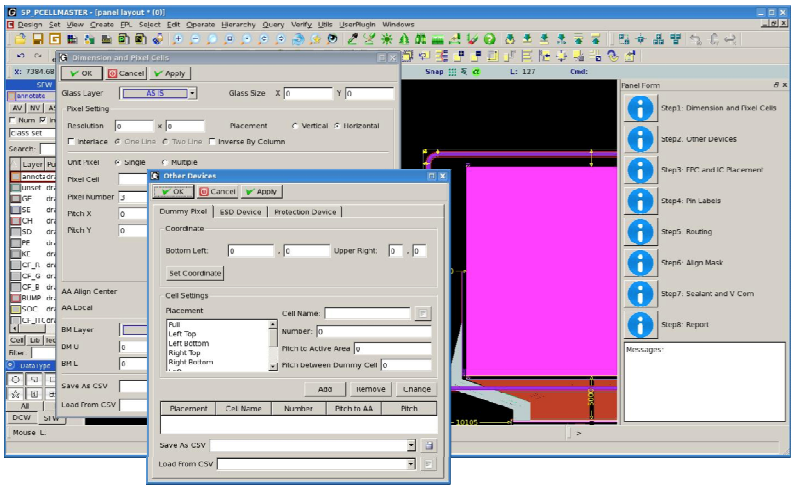
PLAG

Panel Layout Automated Generator

OVERVIEW

PLAG is based on GOLF, a production-proven OpenAccess-based layout platform adopted by world-class semiconductor companies since 2007. PLAG features powerful layout editing functions, intuitive GUI, flexible customization and extension. PLAG provides a versatile layout editor and viewer with simplicity and flexibility. PLAG provides API in C++/TCL/PERL/PYTHON (and more on demand) to help customers develop a variety of applications. PLAG is a cost-effective solution with strong customization support.

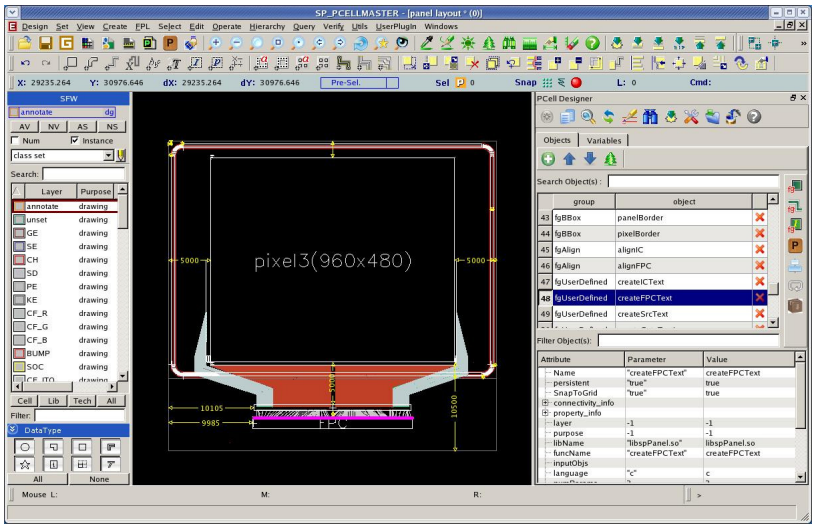
HIGHLIGHTS



- Dynamic viewing: mouse zooming, command viewing
- Selection schemes: mouse select, command select
- Undo and redo
- Auto contact, auto slot
- Array stretch, split, chop
- Bus router
- Equal resistance router
- Resistance measurement
- Hierarchical net tracer
- DRC result viewer
- Data creation: shapes, text, text-array, instance and array, etc.
- Editing: stretch, align, copy, move, transform, append, cut, merge, delete, yank, paste, properties…
- Hierarchical editing: descend, push, EIP, flatten, make cell, etc.
- Query: ruler, distance, measurement, tree, connectivity, trace, etc.
- GUI-based PCell Designer
- PCell-based automated generator for flat panel display layout
- Customized functions: Trim Wire, Print with Exact Size, R/C Loading, Job File Generation, DXF Import/Export, etc.

PCell Designer

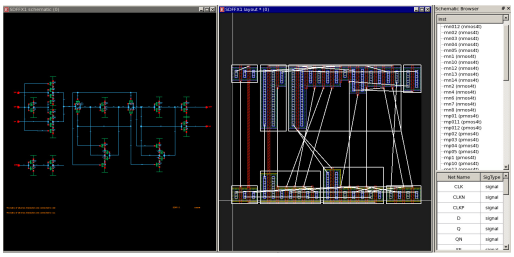
Evolved with the experiences and feedbacks of PCell programmers and layout engineers, PLAG provides a visualized integrated development environment (IDE) for parameterized layout design, preview, testing, debug, and documentation on layout directly. It is based on AnaGlobe's patented highly flexible and reusable hierarchical parameterized layout generator. The OpenAccess (OA) objects of the existing layout can be parameterized directly. More complicated objects such as polygon text, fingers, spiral, and runway are provided. Layout can be composed by geometric operations with object lifetime control. User-defined code (in C++/TCL/PERL/PYTHON) can still be integrated as well.



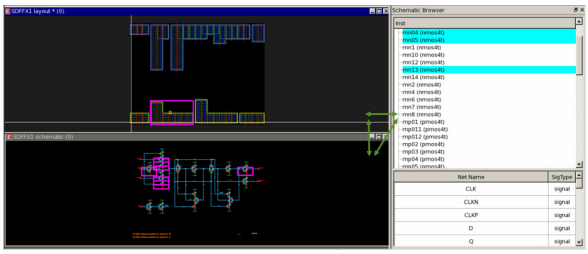
- Program on layout
  - Intuitive GUI-based parameterized layout creation, composition, preview, debugging, testing, and documentation
  - Layout as a sequence of parameterized object evaluations
  - Existing layout can be easily extracted to objects
  - 40+ flexible and reusable object types – from primitive to versatile, all parameterized
  - Step-by-step graphically defined – similar to manual editing
  - Easy to review and debug
  - Maintains design know-how
  - Very easy to craft a variety of automated layout generators
  - Field extensible: supports user-defined objects by C++/TCL/Python/Perl
  - OpenAccess-based: interoperable with any OA-based tools

SCHEMATIC-DRIVEN LAYOUT (SDL)

SDL operates with a hierarchical connectivity model working simultaneously at all levels of the design hierarchy. This capability will alarm connectivity errors as the net is short or open. This makes designers easier to understand the complexity of interactions through the design hierarchy.

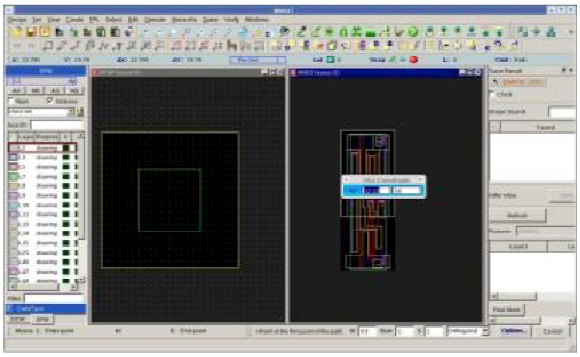


SDL also supports one-to-many mapping across multiple hierarchy levels. This allows layout designers to view different layout hierarchies at the same time for efficient net tracing or debugging. The cross probing of hierarchy net tracer and Short Indicator can easily highlight the problem net without Place-and- Route (P&R), LVS or LPE. It does significantly reduce efforts and speed up the debugging processes.



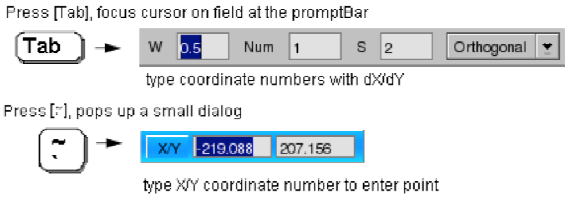
SOPHISTICATED GUI

- Multiple windows management:
  - Layout windows : tile/cascade, bird view review
  - Navigation-based forms: dock/floating
  - Option forms: pop-up/minimized (prompt bar)



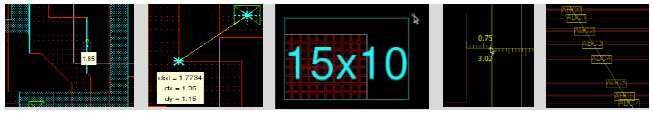
- Comprehensive using style:
  - Layout windows: tile/cascade, bird view review
  - Navigation-based forms: dock/floating
  - Option forms: pop-up/minimized (prompt bar)

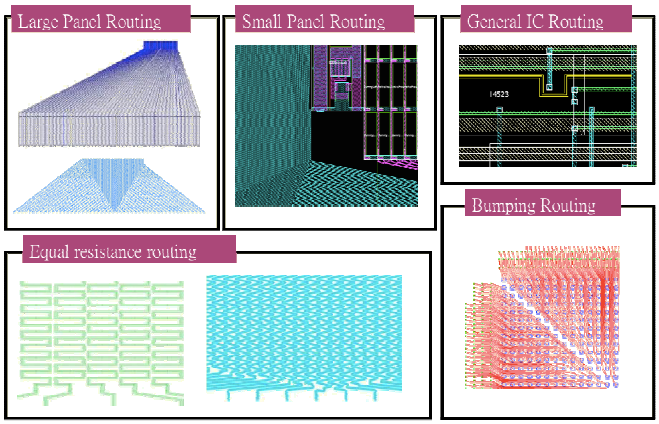
HANDY



EDITING FUNCTIONS

- Align/Abut:
  - Edge to edge, point to point
  - dx/dy offset or Distance mode
  - Multi-to-one alignment (abut)
- Array instance manipulations:
  - Direct stretch
- Rule guide
  - Minimum rules activated snap
- Text array:
  - Irregular pitch supported





CUSTOMIZED ROUTERS FOR FPD LAYOUT

PANEL LAYOUT AUTOMATED GENERATOR

The PLAG solution is the leading technology in flat panel display design and layout. With built-in and customized solution for flat panel layout, PLAG enables FPD designers to create, edit and verify the flat panel design in an integrated and high-performance environment. Following user-defined patterns and parameters, Equal Resistance Route and Bumping Route make fan-in and fan-out connections quickly and accurately.

PLAG provides 8 steps to generate FPD Layout:

1. Dimension and Pixel Cells
2. Other Devices
3. FPC and IC Placement
4. Pin Labels
5. Routing
6. Align Mark
7. Sealant and V Com
8. Report

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