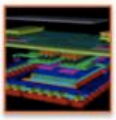
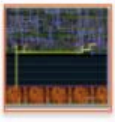
THUNDER™ – Wafer-Level Chip-Scale Layout Integration Platform

OVERVIEW

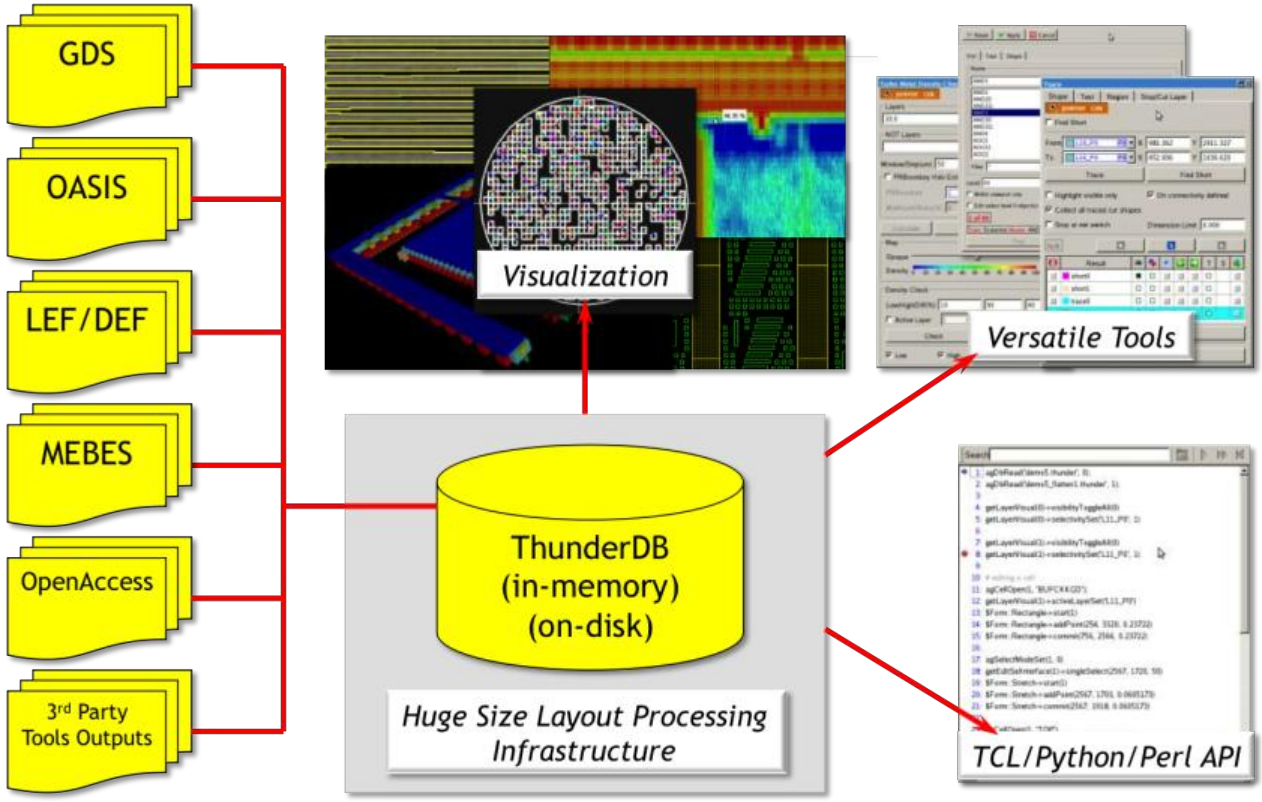
Today's semiconductor industry faces the dynamic nature in either SOC or SIP path-finding and diversity of applications in IoT, automotive, mobile, high performance computing and even heterogeneous components integration. For example, a top-level layout assembly task normally manages hundreds of sub-blocks in either a SOC GPU chip, or an advanced-node testchip design, or a multi-chip SIP project; while each sub-block owner may have many design re-spins. High performance layout integration platform is highly desired to embrace the common challenges in chip-scale, wafer-/panel-level layout integration of complicated design intents, post ECO & dummy engineering, revisions and huge data size and/or with multiple database formats.

THUNDER™ is a versatile layout integration platform to support heavy layout handling efforts from post P&R, IP merge automation & management, physical ECO verification (XOR LVL, connectivity, etc), DRC/LVS debugging interface, and even (in-line inspection) defect-to-layout mapping , failure analysis and chip-package integration (interposer vs. InFO RDL-routing, pins connectivity, etc). ThunderDB is its proprietary database, and is efficient to handle huge layout data with extreme performance of up to 600+GB GDS equivalent per minute. Users can then perform big data analysis for further processing (e.g. 3D-view, cross-section, density mapping, wafer map), machine-learning based optimization, and manipulating data from GDS, OASIS, LEF/DEF, MEBES, OpenAccess and 3rd party tools output.

HIGHLIGHTS

Huge Size Layout		•750+GB Capacity •Hyper Import/Export Performance •Fastest LVL XOR Comparison
IP Merge Automation		•Simple Setup, High Efficiency •Hierarchical and Incremental Merge •Smart Rename
Debugging		•3D Net Tracer •Cross Probing •DRC/LVS Results Analysis (2TB DRC Result Capacity)
Yield Improvement		•Check Density •Patch Dummy •IR Drop Fixing
Failure Analysis		•Voltage Contrast Analysis •FIB Generation •Defects Inspection
Chip-Package Integration		•2.5D/3D Wafer-Level Chip-Scale Packaging Routers •DRC, LVS, Path Tracing •Degassing Holes, Power/Ground Mesh Generation

MAJOR FEATURES



FASTEST LVL COMPARISON

THUNDER™ provides fastest LVL comparison, scalable to data size, with GUI visualization to quickly identify the delta among two designs. Customer benchmarking shows that THUNDER™ LVL consumes the minimal runtime memory, even on industry's biggest chips. (*Fig-1*)

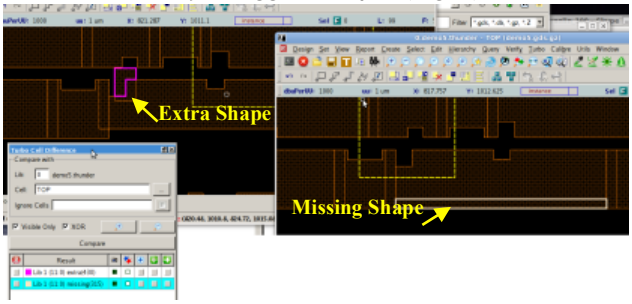


Fig-1. Interactive Layout Comparison

IP MERGE AUTOMATION

THUNDER™ provides system integration for IP from GDS/LEF/DEF files with great flexibility such as standard cell replacement, don't-change list, etc. It performs layout comparison during renaming, which eliminates unnecessary renaming. It supports hierarchical IP merge with incremental change. It generates a summary of missing cells, renamed cells, identical cells, and cross-reference.

BOOLEAN OPERATION

THUNDER™ provides intuitive multiple-Boolean expression to generate shapes on original design directly.

CHIP-SCALE LAYOUT EDITING

THUNDER™ enables user to browse/edit several hundred gigabytes of GDS/OASIS. The intuitive GUI is as friendly as popular layout editors. It provides advanced layout editing features, such as Smart Flatten and snapping to DRC marker, ideal for DRC bug fix.

PHYSICAL NET TRACER

THUNDER™ powerful net tracer provides both tracing and find "shorts", with net highlighting and 3D display visualization. It supports both location based and pin text based tracing. Other debugging functions such as stop layer, net switching detection, and power/ground short detection. (*Fig-2*)

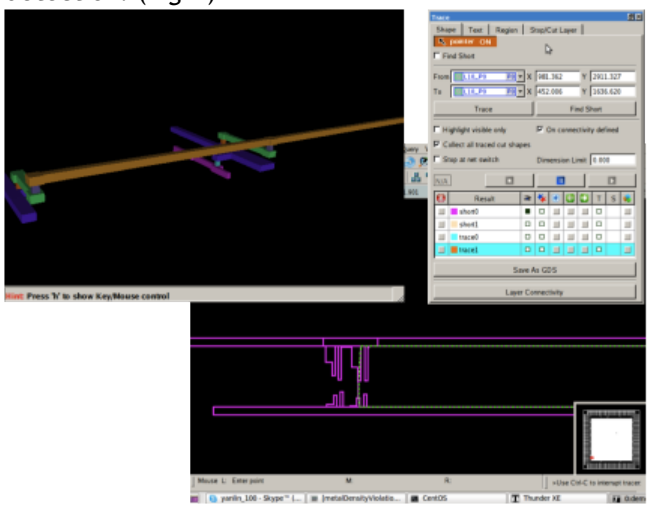


Fig-2. Physical Net Tracer & Short Locator

DENSITY MAP GENERATION & CHECKING

THUNDER™ provides fastest interactive density mapping generation and violation checking with GUI visualization. It provides density variation checking, which is critical for advanced technology nodes. (*Fig-3*)

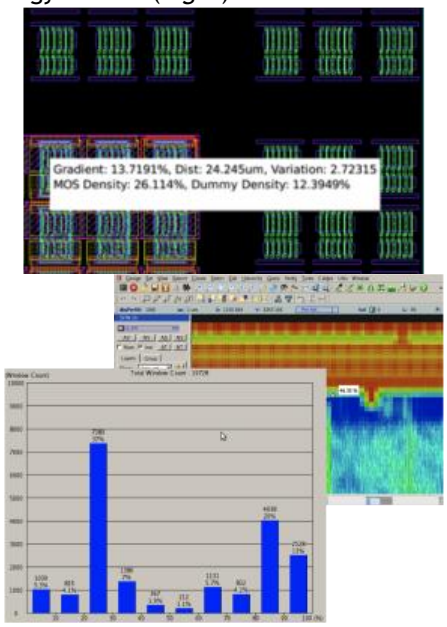


Fig-3. Interactive Density Checking

FAILURE ANALYSIS

THUNDER™ provides a series of functionality to assist the tedious defect inspection job, such as KLA-scanned results viewing, image overlay and extraction, pattern grouping and matching, voltage contrast analysis, FinFET 3D view, cross-section, etc. (*Fig-4*)

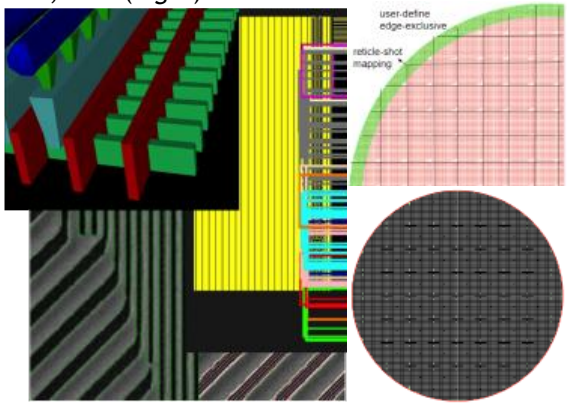


Fig-4. Failure Analysis Related Functionality

HIGHLIGHT MISSING VIAS ON POWER/GROUND NETS

To mitigate the IR-drop issues, THUNDER™ can perform a quick analysis on power/ground nets to highlight areas with missing vias and fix them by inserting vias. (*Fig-5*)

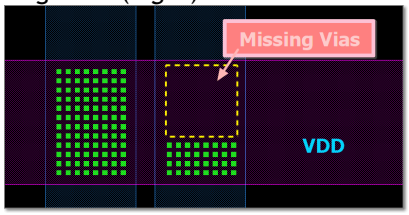


Fig-5. Fix Missing Vias

HUGE CAPACITY DRC/LVS/DEFECT EXPLORER

THUNDER™ provides seamless integration with 3rd party layout verification and wafer inspection tools. It helps the user to navigate and debug huge number of DRC/LVS errors and defects efficiently (handles 2+TB DRC results). It also supports Calibre short isolation result with 3D display and cross probing. (*Fig-6*)

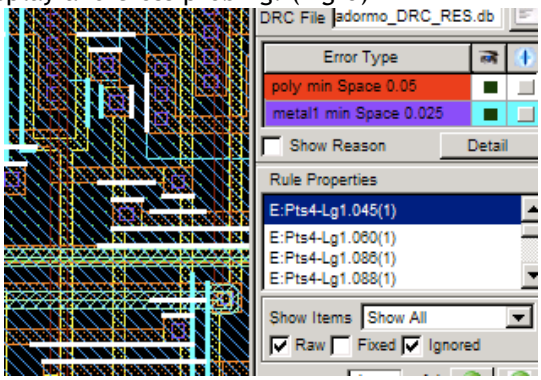


Fig-6. DRC Result Viewer

DUMMY FILL PATCHING

THUNDER™ can fill dummy patterns to low density area interactively with target percentage. It creates vertical/horizontal patterns with offset. It can also take Calibre DRC marker as the target area. (*Fig-7*)

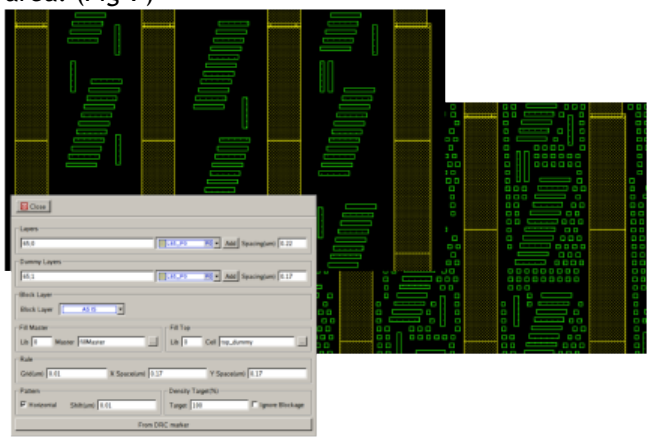


Fig-7. Interactive Dummy Fill Patching

2.5D PACKAGING INTERPOSER ROUTER

THUNDER™ provides the industry's first dedicated interposer router for 2.5D packaging. It provides a unified routing framework that can handle both grid-based and gridless routing on RDLs. (*Fig-8*)

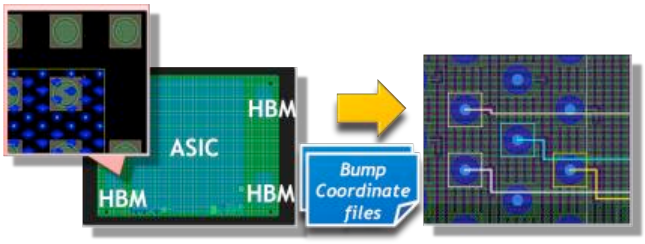


Fig-8. Interposer Routing for 2.5D Packaging

THUNDER™ Feature Summary

	View GLV	Basic Editing BLE	Extreme Editing XLE	Packaging add on WLP	MEBES add on MBS	Turbo add on TBO
GDS, OSSIS, LEF/DEF, OpenAccess	●	●	●			
MEBES reader					●	
ThunderDB	read	read/write	read/write			
Layout Viewing	●	●	●			
Layout Editing		●	●			
IP Merge						
Interactive merge		●	●			
Project-based merge		●	●			
Stream-line merge		●	●			
Save merge		●	●			
Library consolidation		●	●			
Verification						
Density check	●	●	●			accelerated
ECO LVL/XOR		●	●			accelerated
Debugging						
Net trace	●	●	●			
DRC/LVS result view	●	●	●			
3D view, 2D cross-section	●	●	●			
Calibre & ICV interface	●	●	●			
Wafer Inspection						
Overlay (layout/layout, layout/mage)	●	●	●			
FIB generation			●			
Voltage contrast analysis			●			
Pattern matching/grouping						●
Image contour to layout recognition			●			
Utilities						
Trim ECO dummy			●			
Dummy patching		●	●			
Multiple Boolean operations			●			
Measure resistance		●	●			
Scripting						
Python/TCL/Perl support	●	●	●			
ThunderDB API			●			
User form	●	●	●			
User menu	●	●	●			
TK GUI	●	●	●			
Chip-Package Integration						
InFO RDL router				●		
Interposer RDL router				●		
Interactive pin-to-pin router				●		
DRC/LVS				●		
Utilities (degassing holes, path tracing, etc.)				●		
DB conversion (DXF)				●		

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