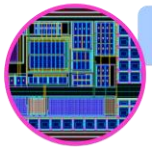
AnaGlobe

GOLF – Custom Layout Platform with Patented PCell Design and Test Structure

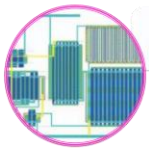
OVERVIEW

GOLF is a production-proven OpenAccess-based layout platform adopted by world-class scompanies of fabless design, layout and design service, semiconductor foundries and flat panel display manufacturers. GOLF features powerful layout viewing and editing functions, intuitive GUI, flexible customization and more extension, with both simplicity in GUI and flexibility in design flows. Its API with C++/TCL/PERL/PYTHON interface (and more on demand) helps users developing a variety of applications. GOLF capabilities facilitate great customization for different applications, such as custom layout functions, analog layout automation (schematic or constraint-driven layout, etc), testchip structure layout automation (from PCell designer to IP block/component and to chip-level layout) or panel-level layout integration and automation.



Custom Layout

- **Intuitive GUI, Advanced Functions**
- **Multiple Patterning, FinFET Grid**
- FinFET Transistor Level Placer
- **ECO Comparison**



Analog Layout Automation

- **Schematic-Driven Layout**
- **Constraint-Driven Analog Placer & Router**
- Parasitic-Aware Capacitor Placer & Router
- Learning-Based Analog Layout Assistant

Test Structure Layout Automation

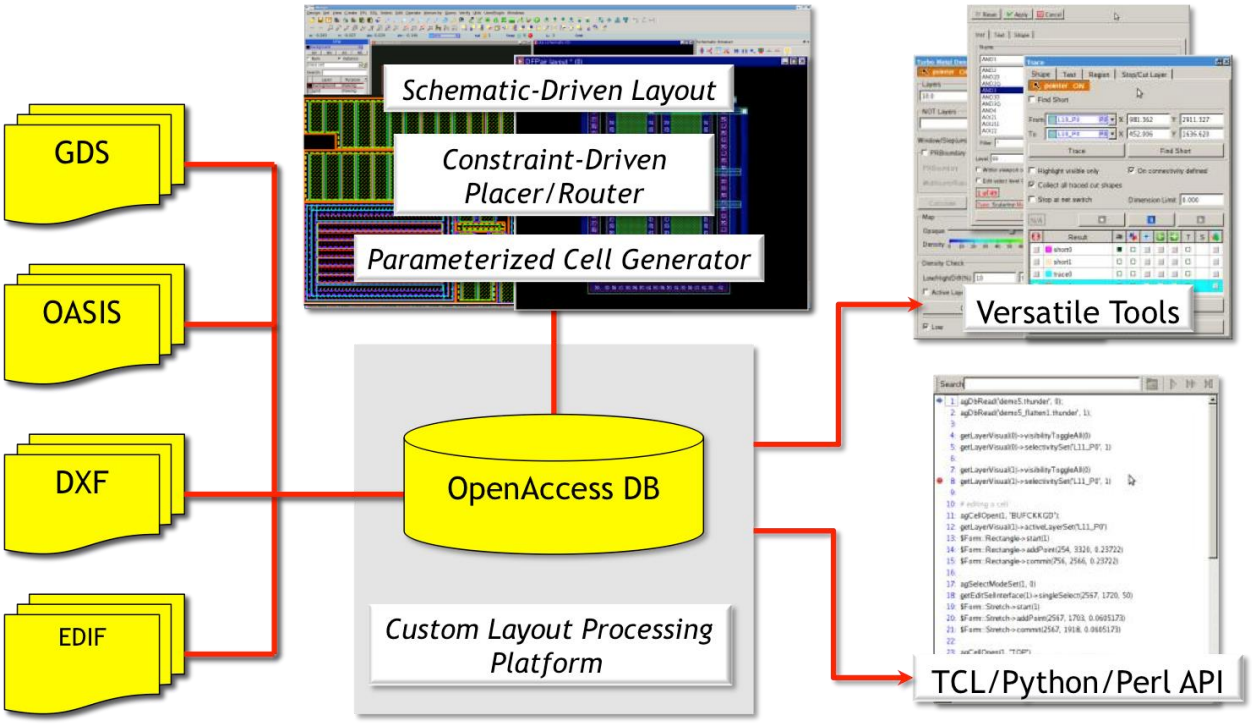
- **PCell Designer**
- **Test Module Generator**
- **Test Structure Assembler**
- Configurable & Reusable Flow

Flat Panel Display Layout Automation

- **Fanout Router & WOA Router**
- Free-Form Array Cutting
- Free-Form Fanout Region Router
- Any-Angle Cell Instance/Array Rotation

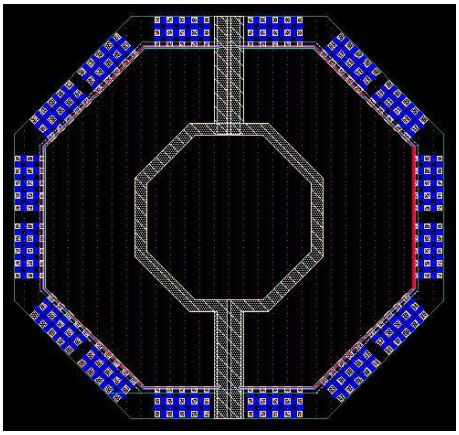
GUI HIGHLIGHTS

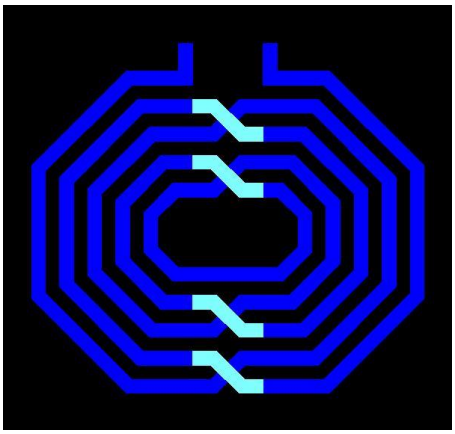
- Auto contact, auto slot
- Array stretch, split, chop
- Undo and redo
- Layout windows: tile/cascade, bird view
- Navigation-based forms: dock/floating
- Option forms: pop-up/minimized (prompt bar)
- Dynamic viewing: mouse zooming, command viewing
- Selection schemes: mouse select, command select
- Data creation: shapes, text, text-array, instance and array…
- Editing: stretch, align, copy, move, transform, append, cut, merge, delete, yank, paste, properties…
- Hierarchical editing: descend, push, EIP, flatten, make cell…
- Query: ruler, distance, measurement, tree, connectivity, trace…
- Verify: Calibre DRC/LVS results viewer, run Calibre DRC/LVS/RVE, IC Validator VUE Interface
- Built-in hierarchical schematic viewer

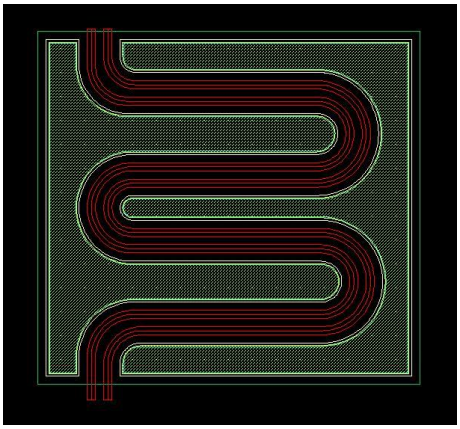


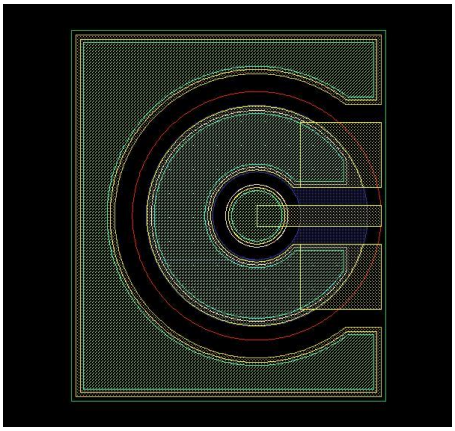
PCELL DESIGNER

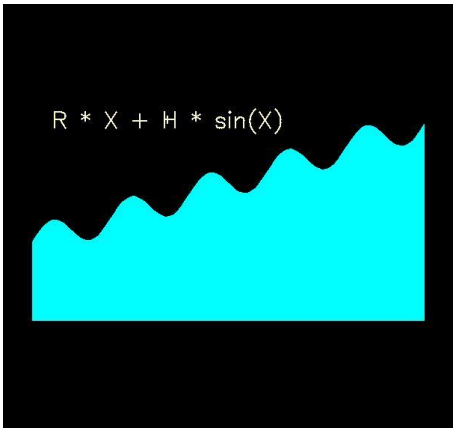
Evolved with the experiences and feedbacks of PCell programmers and layout engineers, GOLF provides a visualized integrated development environment (IDE) for parameterized layout design, preview, testing, debug, and documentation on layout directly. It is based on AnaGlobe's patented highly flexible and reusable hierarchical parameterized layout generator. The OpenAccess (OA) objects of the existing layout can be parameterized directly. More complicated objects such as polygon text, fingers, spiral, and runway are provided. Layout can be composed by geometric operations with object lifetime control. User-defined code (in C++/TCL/PERL/PYTHON) can still be integrated as well.

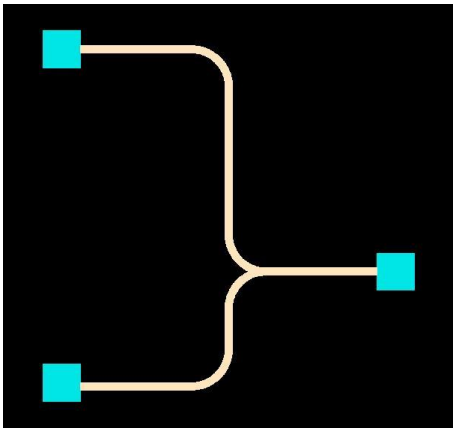






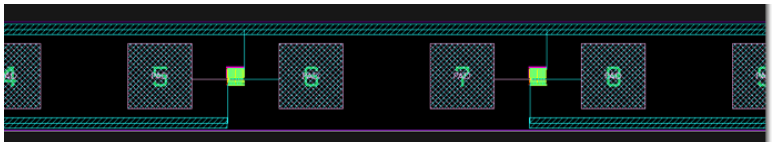




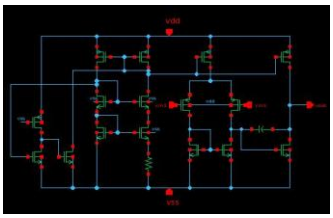


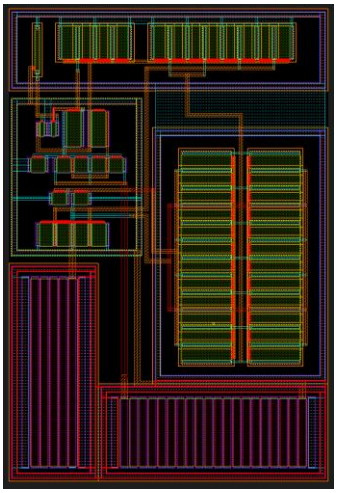
TEST STRUCTURE LAYOUT AUTOMATION

- Interactive test modules generation
- Friendly straight-forward flow:
  - ✧ User-configured probe-lines (pad, slots, label and routing)
  - ✧ Excel split table driven auto layout
  - ✧ Test modules generation



SCHEMATIC-DRIVEN LAYOUT (SDL)





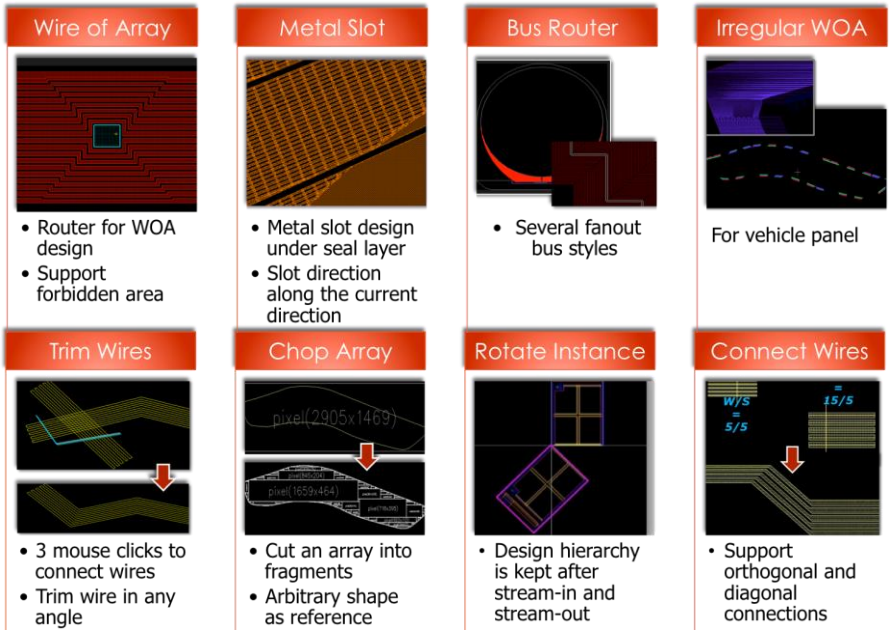
GOLF SDL operation honors a hierarchical connectivity model working simultaneously at all levels of hierarchy. This facilitates designers aware of the complexity of interactions through full design hierarchy, and supports one-to-many mapping across multiple hierarchy levels. For example, GOLF will alarm connectivity errors if a net is short or open; layout designers to view different layout hierarchies at the same time for efficient net tracing or debugging. Such cross-probing of hierarchical net-tracer and Short-indicator can easily highlight the problematic nets, significantly reduce efforts and speed up the debugging efforts.

- Layout realization from schematic using PCell devices
- Transistor/Resistor/Capacitor/Inductor PCell mapping
- Mapping from predefined sub-circuit layout
- Analog placer with multiple constraints: Symmetry, Proximity, Preplaced, Fixed-Boundary-Block, Boundary, Minimum Separation
- Analog router with multiple constraints: Symmetry, Topology-Matching, Length-Matching, Length-Ratio-Matching, Bounding
- Supports PCell transistors merge/split/stretch/folding functions
- Cross-probing between schematic/layout and netlist browser
- Connectivity driven editing: net propagation when creating wire, net flylines, real-time short and open detection
- Schematic comparison in ECO flow

FLAT PANEL DISPLAY LAYOUT AUTOMATION

GOLF provides leading edge solution for flat panel display layout:

- Fanout routers: pattern router and equal-resistance router
- WOA router: Wire on array router with constraints, rules, boundary selection, pin assignment and forbidden area selection
- Slot Metal: Generate slots (holes) on any angle irregular polygons
- Automated layout generator: Dimension and Pixel Cells, Dummy Pixel, ESD and Protection Devices, FPC and IC Placement, Pin Labels, Routing, Align Mark, Sealant and V Com, Report
- Customized functions: Mask Splitter, Job File, ASP Report Coordinate, RC Loading, Mother Glass Splitter, Cell Overlap Check, TP Stitching



AnaGlobe

AnaGlobe Technology, Inc.
615R, Innovation & Incubation Hall, Tsing Hua University
No.101, Sec. 2, Kuang-Fu Road
Hsinchu 30013, Taiwan
Phone: +886-3-5613650
Email: sales@anaglobe.com
http://www.anaglobe.com