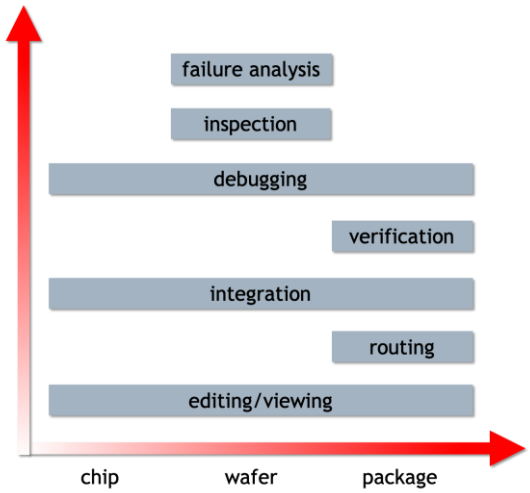
AnaGlobe

THUNDER - Wafer-Level Chip-Scale Integration Applications Framework

OVERVIEW

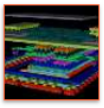
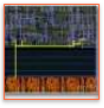


Today's semiconductor industry faces the dynamic nature in either SOC or SIP path-finding and diversity of applications in IoT, automotive, mobile, high performance computing and even heterogeneous components integration. For example, a top-level layout assembly task normally manages hundreds of sub-blocks in either a SOC GPU chip, or an advanced-node testchip design, or a multi-chip SIP project; while each sub-block owner may have many design re-spins.

High performance layout integration platform is highly desired to embrace the common challenges in chip-scale, wafer-/panel-level layout integration of complicated design intents, post ECO & dummy engineering, revisions and huge data size and/or with multiple database formats.

THUNDER is a versatile layout integration platform to support heavy layout handling efforts from post P&R, IP merge automation & management, physical ECO verification (XOR LVL, connectivity, etc.), DRC/LVS debugging interface, and even (in-line inspection) defect-to-layout mapping, failure analysis and chip-package integration (Fanout RDL, interposer and Substrate routing, pins connectivity, etc.). ThunderDB is its proprietary database, and is efficient to handle huge layout data with extreme performance of up to 600+GB GDS equivalent per minute. Users can then perform big data analysis for further processing (e.g. 3D-view, cross-section, density mapping, wafer map), machine-learning based optimization, and manipulating data from GDS, OASIS, LEF/DEF, MEBES, OpenAccess, as well as 3rd party tools output.

MAJOR FEATURES

Huge Size Layout Review		•*Terabytes Capacity* •*Hyper Import/Export Performance* •*Fastest LVL XOR Comparison*
IP Integration		•*Simple Setup, High Efficiency* •*Hierarchical and Incremental Merge* •*Smart Rename*
Debugging		•*3D Net Tracer/Multiple Net Tracer* •*Cross Probing* •*DRC/LVS Results Analysis*
Yield Improvement		•*Check Density* •*Patch Dummy* •*IR Drop Fixing*
Failure Analysis		•*Voltage Contrast Analysis* •*FIB Generation* •*Defects Inspection*
Chip-Package Integration		•*2.5D/3D Wafer-Level Chip-Scale Packaging Routers* •*LVS, Path Tracing* •*Degassing Holes, Power/Ground Mesh Generation*

FASTEST LVL COMPARISON

THUNDER provides fastest LVL comparison, scalable to data size, with GUI visualization to quickly identify the delta among two designs. Customer benchmarking shows that THUNDER LVL consumes the minimal runtime memory, even on industry's biggest chips. (*Fig-1*)

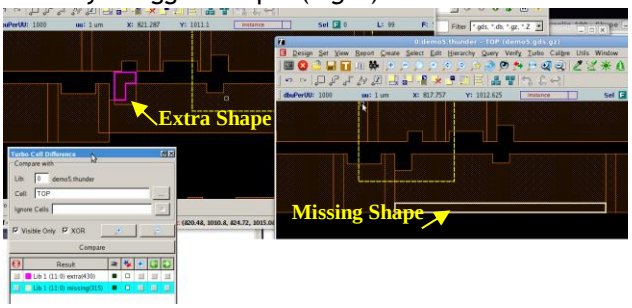


Fig-1. Interactive Layout Comparison

MARK VIEW

THUNDER provides a "SNAPSHOT" feature and supports to take jpg images based on Mark View points as center with user specified dimension. The "Auto Measure" option adds ruler of shortest distance on the image. In addition, A Multi-Thread feature is added to better perform large quantity images. (*Fig-2*)

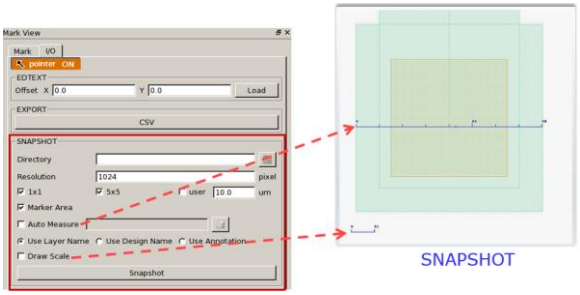


Fig-2. Snapshot

LAYERS OVERLAY

THUNDER provides users to overlay several selected GDS/OASIS files and shows the overlap area with different color. (*Fig-3*)

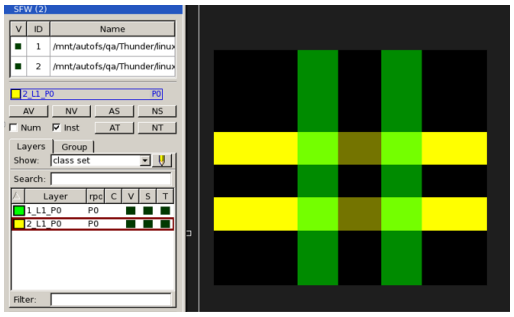


Fig-3. Layers Overlay

CHIP-SCALE LAYOUT EDITING

THUNDER enables user to browse/edit several hundred gigabytes of GDS/OASIS. The intuitive GUI is as friendly as popular layout editors. It provides advanced layout editing features, such as Smart Flatten and snapping to DRC marker, ideal for DRC bug fix.

BOOLEAN OPERATION

THUNDER provides intuitive multiple-Boolean expression to generate shapes on original design directly.

IP MERGE AUTOMATION

THUNDER provides system integration for IP from GDS/LEF/DEF files with great flexibility such as standard cell replacement, don't-change list, etc. It performs layout comparison during renaming, which eliminates unnecessary renaming. It supports hierarchical IP merge with incremental change. It generates a summary of missing cells, renamed cells, identical cells, and cross-reference.

PHYSICAL NET TRACER/FAST TRACE/MULTIPLE TACER

THUNDER powerful net tracer provides both tracing, multiple tracing and finding "shorts", with net highlighting and 3D display visualization. It supports both location based and pin text based tracing, and even grouping layers connectivity (identity layers: multi-pattern layers, dummy layers). Other debugging functions such as stop layer, net switching detection, and power/ground short detection. (*Fig-4*)

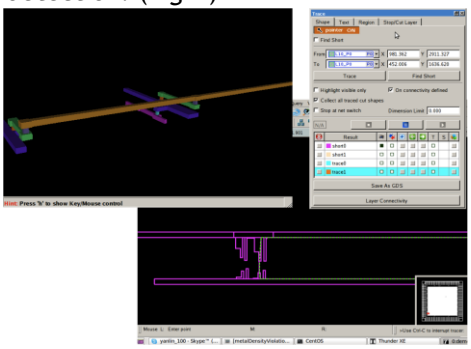


Fig-4. Physical Net Tracer & Short Locator

DENSITY MAP GENERATION & CHECKING

THUNDER provides the fastest interactive density mapping generation and violation checking with GUI visualization. It provides density variation checking, which is critical for advanced technology nodes. (*Fig-5*)

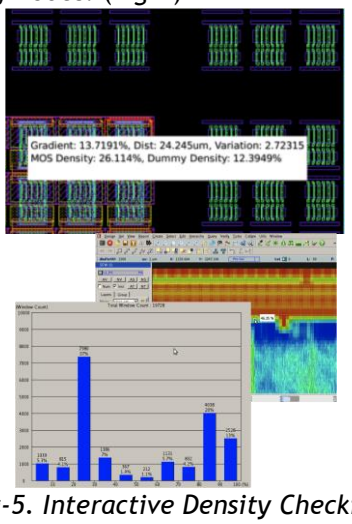


Fig-5. Interactive Density Checking

FAILURE ANALYSIS

THUNDER provides a series of functionality to assist the tedious defect inspection job, such as KLA-scanned results viewing, image overlay and extraction, pattern grouping and matching, voltage contrast analysis, FinFET 3D view, cross-section, etc. (*Fig-6*)

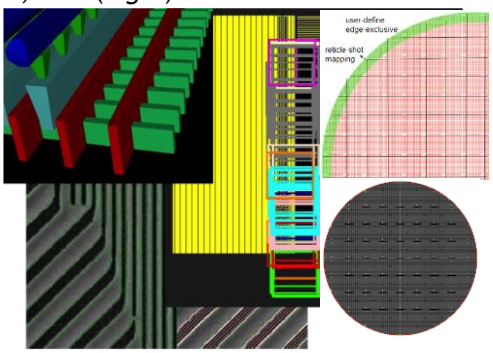


Fig-6. Failure Analysis Related Functionality

HUGE CAPACITY DRC/LVS/DEFECT EXPLORER

THUNDER provides seamless integration with 3rd party layout verification and wafer inspection tools. It helps the user to navigate and debug huge number of DRC/LVS errors and defects efficiently (handles 2+TB DRC results). It also supports Calibre short isolation result with 3D display and cross probing. (*Fig-7*)

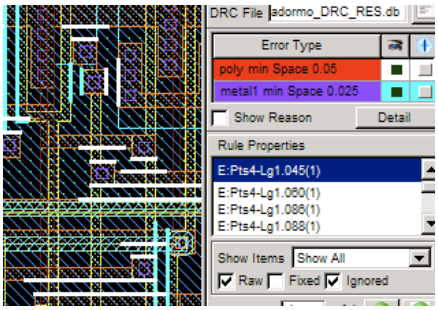


Fig-7. DRC Result Viewer

HIGHLIGHT MISSING VIAS ON POWER/GROUND NETS

To mitigate the IR-drop issues, THUNDER can perform a quick analysis on power/ground nets to highlight areas with missing vias and fix them by inserting vias. (*Fig-8*)

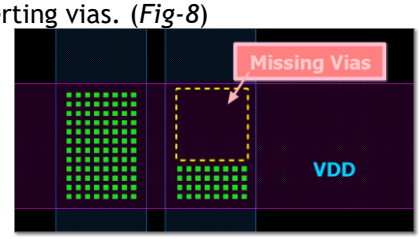


Fig-8.Fix Missing Vias

DUMMY FILL PATCHING

THUNDER can fill dummy patterns to low density area interactively with target percentage. It creates vertical/horizontal patterns with offset. It can also take Calibre DRC marker as the target area. (*Fig-9*)

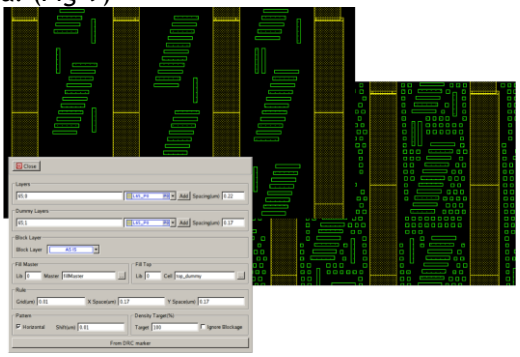


Fig-9. Interactive Dummy Fill Patching

SiP INTEGRATION

THUNDER provides the industry's first integrated router for SiP. It provides a unified routing framework to handle from Fanout RDL, Interposer to Substrate. It also provides a rich set of functions for chip-package integration such as power distribution network, shielding, degassing hole, wirebond planning, connectivity checking and design rule checking.

POWERFUL SCRIPTING

THUNDER supports db-level API in Perl/Tcl/ Python with a built-in debugger.

LIB CONSOLIDATION

THUNDER can consolidate duplicated layouts to reduce the file size. (*Fig-10*)

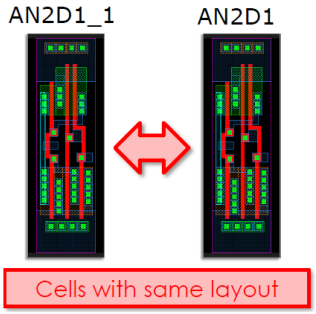


Fig-10. Cells Comparison

CACHE BROWSER

THUNDER provides a friendly GUI to manage cache files.

THUNDER DEFECT DRC

THUNDER helps the foundry users to investigate the root cause of defect much more efficiently.

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