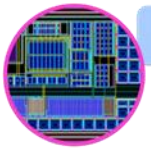
AnaGlobe

# GOLF – Custom Layout Platform with Patented PCell Design and Test Structure

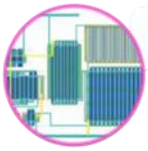
## OVERVIEW

GOLF is a production-proven OpenAccess-based layout platform adopted by world-class scompanies of fabless design, layout and design service, semiconductor foundries and flat panel display manufacturers. GOLF features powerful layout viewing and editing functions, intuitive GUI, flexible customization and more extension, with both simplicity in GUI and flexibility in design flows. Its API with C++/TCL/PERL/PYTHON interface (and more on demand) helps users developing a variety of applications. GOLF capabilities facilitate great customization for different applications, such as custom layout functions, analog layout, testchip structure layout automation (from PCell designer to IP block/component and to chip-level layout).



### Custom Layout

- **Intuitive GUI, Advanced Functions**
- **Multiple Patterning, FinFET Grid**
- FinFET Transistor Level Placer
- **ECO Comparison**



### Analog Layout

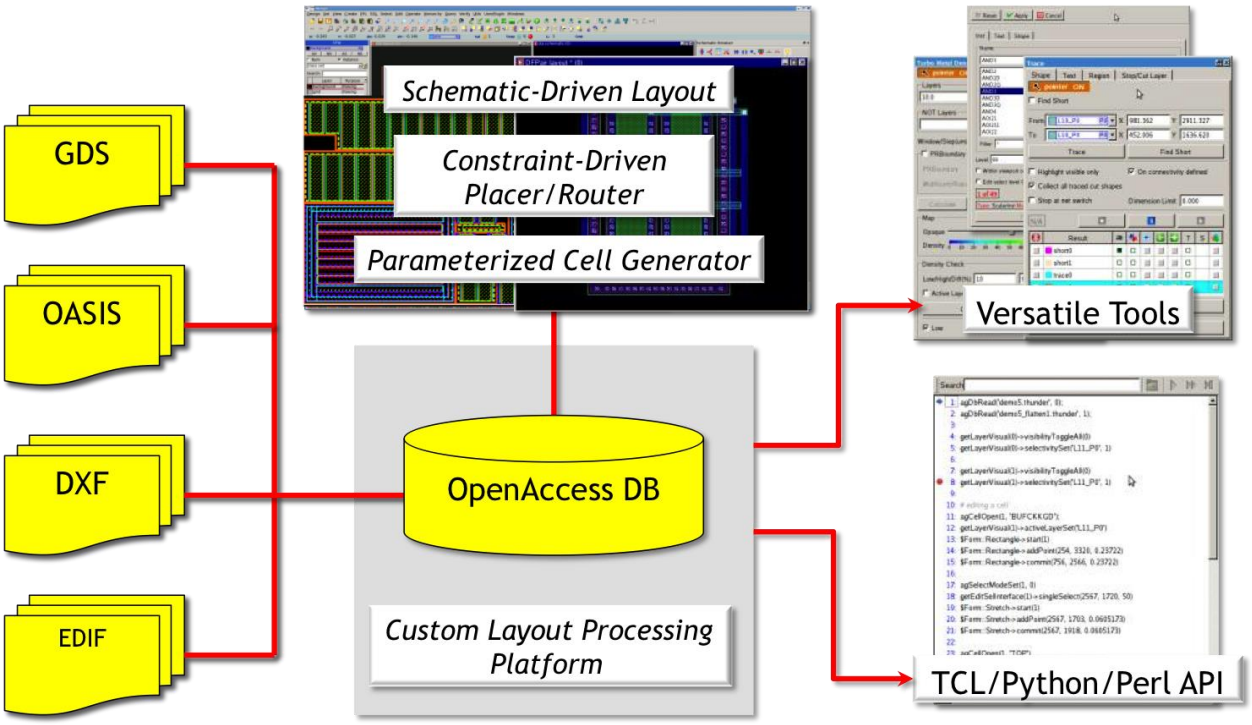
- **Constraint-Driven Analog Placer & Router**
- Parasitic-Aware Capacitor Placer & Router
- Learning-Based Analog Layout Assistant

### Test Structure Layout Automation

- **PCell Designer**
- **Test Module Generator**
- **Test Structure Assembler**
- Configurable & Reusable Flow

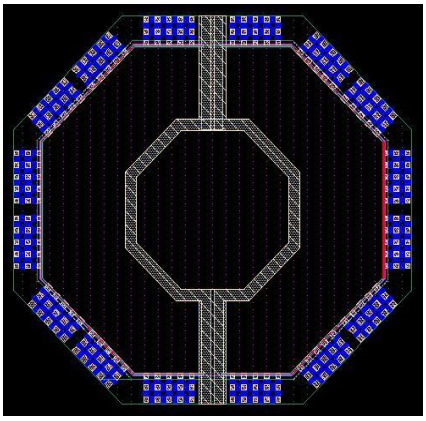
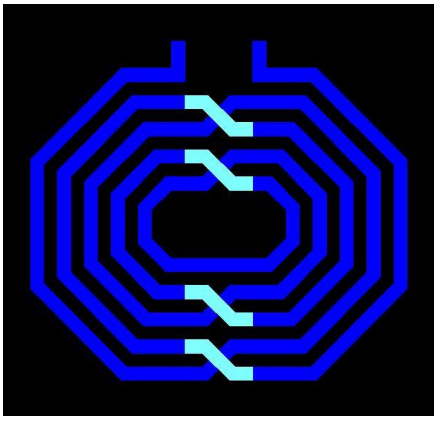
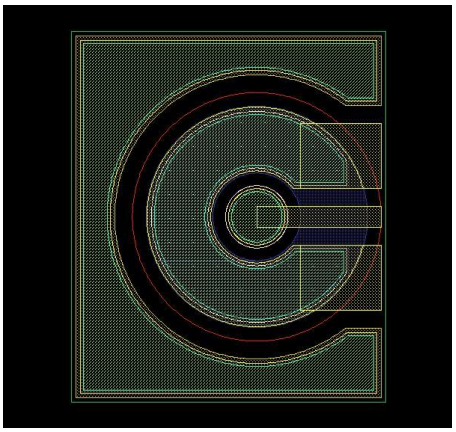
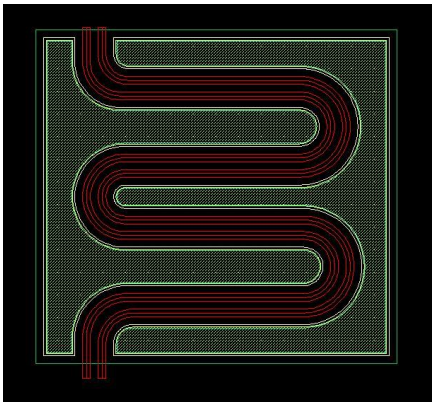
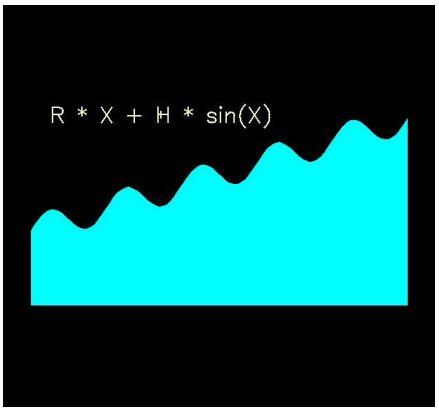
## GUI HIGHLIGHTS

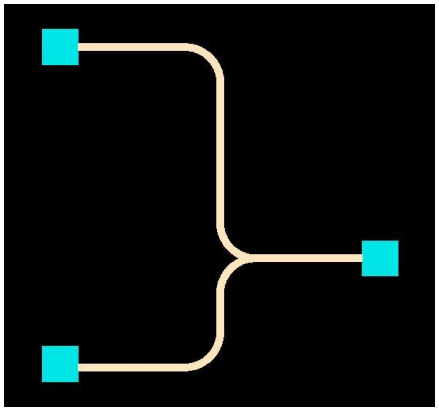
- Auto contact, auto slot
- Array stretch, split, chop
- Undo and redo
- Layout windows: tile/cascade, bird view
- Navigation-based forms: dock/floating
- Option forms: pop-up/minimized (prompt bar)
- Dynamic viewing: mouse zooming, command viewing
- Selection schemes: mouse select, command select
- Data creation: shapes, text, text-array, instance and array…
- Editing: stretch, align, copy, move, transform, append, cut, merge, delete, yank, paste, properties…
- Hierarchical editing: descend, push, EIP, flatten, make cell…
- Query: ruler, distance, measurement, tree, connectivity, trace…
- Verify: Calibre DRC/LVS results viewer, run Calibre DRC/LVS/RVE, IC Validator VUE Interface
- Built-in hierarchical schematic viewer



## PCELL DESIGNER

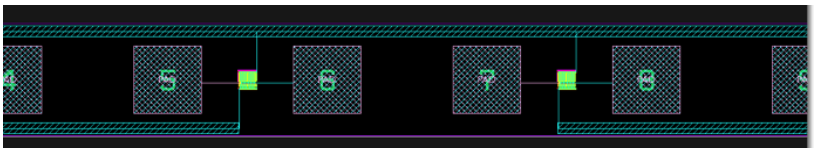
Evolved with the experiences and feedbacks of PCell programmers and layout engineers, GOLF provides a visualized integrated development environment (IDE) for parameterized layout design, preview, testing, debug, and documentation on layout directly. It is based on AnaGlobe's patented highly flexible and reusable hierarchical parameterized layout generator. The OpenAccess (OA) objects of the existing layout can be parameterized directly. More complicated objects such as polygon text, fingers, spiral, and runway are provided. Layout can be composed by geometric operations with object lifetime control. User-defined code (in C++/TCL/PERL/PYTHON) can still be integrated as well.



## TEST STRUCTURE LAYOUT AUTOMATION

- Interactive test modules generation
- Friendly straight-forward flow:
  - ✧ User-configured probe-lines (pad, slots, label and routing)
  - ✧ Excel split table driven auto layout
  - ✧ Test modules generation




AnaGlobe

AnaGlobe Technology, Inc.
615R, Innovation & Incubation Hall, Tsing Hua University
No.101, Sec. 2, Kuang-Fu Road
Hsinchu 30013, Taiwan
Phone: +886-3-5613650
Email: sales@anaglobe.com
http://www.anaglobe.com